REMARKS

Claims 17 and 20-44 remain in this application. Claims 18-19 have been cancelled without prejudice. Claims 17, 20-24, 26-27, and 29 have been amended to more properly define the invention. The amended claims are supported by the specification. Claims 30-44 have been added. No new matter has been added. The Applicants respectfully request reconsideration of this application in view of the above amendments and the following remarks.

35 U.S.C. §102 Rejection - Usami

The Examiner has rejected claims 17 and 18 under 35 U.S.C. §102 as being anticipated by U.S. Patent No. 6,222,269 issued to Usami (hereinafter referred to as "Usami").

Claim 17 as amended recites, "*patterning the mask layer such that the first and second **power** interconnect lines and a first portion of the patterned first layer are **covered**, and the third and fourth **signal** interconnect lines and a second portion of the patterned first layer are **uncovered***", and "*depositing a second layer of a second dielectric material between the third and fourth signal interconnect lines, the second dielectric material having a smaller dielectric constant than the first dielectric material*".

Applicants request reconsideration of this rejection because Usami does not teach or suggest: (1) power lines, (2) patterning such that power lines are covered and signal lines are uncovered, or (3) depositing a smaller dielectric constant material between signal lines than between power lines.

First, Usami does not teach or suggest power lines. Usami only discusses signal carrying interconnect lines (see for example column 5, lines 22-25).

Second, Usami does not teach or suggest patterning such that power lines are covered and signal lines are uncovered. Rather, Usami discusses forming insulators between signal carrying interconnect lines based on **spacing distances** between the signal carrying interconnect lines. See for example column 3, lines 13-22. This is also shown in Figure 3A in that the resist mask 14 covers the widely-spaced region as discussed at column 7, lines 12-17 as follows:

> "As illustrated in FIG. 3(a), resist masks are then formed so as to **expose** a portion of the first interlevel insulator 4 in a **narrowly-spaced** region between adjacent interconnect lines but to **cover** another portion of the first insulating layers 4 in a **widely-spaced** region between adjacent interconnect lines, in lower interconnect lines 3 of damascene interconnection."

Rather than patterning based on the electrical nature of the interconnects, namely whether they carry power or signals, Usami takes a different approach that is based on spacing distance between the interconnect lines due to mechanical considerations associated with the spacing distances. The two mechanical considerations discussed in Usami are strength and coefficient of thermal expansion. This is further discussed at column 3, lines 13-22:

> "In addition, an interlevel insulator having a small coefficient of thermal expansion and high strength is used in a widely-spaced region between interconnect lines, which makes it possible to overcome the problem of crack generation in an interlevel insulator which would take place when a low-dielectric-constant insulating layer is used in all the regions as an interlevel insulator."

Accordingly, Usami does not teach or suggest patterning such that power lines are covered and signal lines are uncovered but rather takes a different approach based on

forming resist masks based on spacing distances between the lines and mechanical properties of the insulation materials.

Third, Usami does not teach or suggest depositing a smaller dielectric constant material between signal lines than between power lines. Without limitation, as discussed in the patent application, this may be done for electrical reasons to provide relatively high valued decoupling capacitors between power supply lines while providing low parasitic capacitance between signal lines (e.g., see application page 7). Usami does not discuss decoupling capacitance or provide any other suggestion or motivation for depositing in the way claimed.

Accordingly, claim 17 is believed to be allowable. **Claim 30** depends from claim 17 and is believed to be allowable therefor as well as for the recitations independently set forth therein.

35 U.S.C. §103(a) Rejection - Usami

The Examiner has rejected claims 19, 23-30 under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 6,222,269 issued to Usami (hereinafter referred to as Usami".

Claim 23 as amended recites, "*forming a first plurality of conductive power lines ... having a first dielectric therebetween", "forming a second plurality of conductive signal lines ... having a second dielectric therebetween", and "wherein the first dielectric has a dielectric constant greater than a dielectric constant of the second dielectric*". Usami does not teach or suggest these limitations. Accordingly, claim 23 is believed to be allowable. **Claim 34** depends from claim 23 and is believed to be allowable therefor as well as for the recitations independently set forth therein.

Claim 24 as amended recites, "*forming a second plurality of power interconnect lines in the second intralayer dielectric*". Usami does not teach or suggest these limitations. Accordingly, claim 24 is believed to be allowable. **Claims 25-26 and 35-36** depend from claim 24 and are believed to be allowable therefor as well as for the recitations independently set forth therein.

Claim 27 as amended recites, "*forming a plurality of signal lines in the first dielectric layer and a power line in the second dielectric layer*". Usami does not teach or suggest these limitations. Accordingly, claim 27 is believed to be allowable. **Claims 28-29 and 37** depend from claim 27 and are believed to be allowable therefor as well as for the recitations independently set forth therein.

35 U.S.C. §103(a)Rejection – Usami in view Cho

The Examiner has rejected claims 20-22 under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 6,222,269 issued to Usami (hereinafter referred to as "Usami") in view of U.S. Patent No. 5,512,775 issued to Cho ("Cho").

Claim 20 as amended recites, "*forming a first pair of power interconnect lines to distribute power and a second pair of signal interconnect lines to carry signals from the conductive material*" and "*patterning the mask layer such that one portion of the dielectric material between one pair is covered and another portion of the dielectric material between another pair is uncovered*". Usami does not teach or suggest these limitations. Additionally, the limitations not taught by Usami are also not taught by Cho.

Accordingly, claim 20 is believed to be allowable. **Claims 21-22 and 31-33** depend from claim 20 and are believed to be allowable therefor as well as for the recitations independently set forth therein.

Conclusion

Applicant respectfully submits that the rejections have been overcome by the amendment and remark, and that the claims as amended are now in condition for allowance. Accordingly, Applicant respectfully requests the rejections be withdrawn and the claims as amended be allowed. The Examiner is requested to call Brent E. Vecchia at (303) 740-1980 if there remains any issue with allowance of the case.

Request For An Extension Of Time

The Applicant respectfully petitions for an extension of time to respond to the outstanding Office Action pursuant to 37 C.F.R. § 1.136(a) should one be necessary. Please charge our Deposit Account No. 02-2666 to cover the necessary fee under 37 C.F.R. § 1.17 for such an extension.

Charge Our Deposit Account

Please charge any shortage to our Deposit Account No. 02-2666.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

Date: _____

_____
Brent E. Vecchia
Reg. No. 48,011

12400 Wilshire Boulevard
Seventh Floor
Los Angeles, California 90025-1030
(303) 740-1980

VERSION WITH MARKINGS TO SHOW CHANGES MADE

In The Specification:

The paragraph beginning at page 14, line 6 has been amended as follows:

Fig. 17 is a schematic cross-section showing a patterned masking layer **406** over a first dielectric material **404**, which, in turn, is disposed over a substrate **402**. In the illustrative embodiment, substrate **402** is a wafer with various electrical components, interconnections, and insulating regions formed therein. First dielectric [**406**] **404** is any suitable material with a dielectric constant greater than or equal to the dielectric constant of silicon dioxide. Barium strontium titinate (BST) is one example of a high-k material.

In The Claims:

The claims have been amended as follows:

17. (Amended) A method of forming an interconnect structure, comprising:

forming a first layer of a first dielectric material on a substrate;

patterning the first layer;

depositing conductive material over the patterned first layer;

planarizing the conductive material such that a plurality of interconnect lines are formed including a first and a second power interconnect lines and a third and fourth signal interconnect lines;

forming a mask layer over the interconnect lines and patterned first layer;

patterning the mask layer such that the first and second power interconnect lines and a first portion of the patterned first layer are covered, and the third and fourth

signal interconnect lines and a second portion of the patterned first layer are uncovered [a first portion of the interconnect lines and patterned first layer are covered, and a second portion of the interconnect lines and patterned first layer are uncovered];

removing the dielectric material from the uncovered portion;

removing the second portion of the patterned first layer [the patterned mask layer]; and

depositing a second layer of a second dielectric material between the third and fourth signal interconnect lines, the second dielectric material having a smaller dielectric constant than the first dielectric material.

20. (Amended) A method of forming an interconnect structure, comprising:

forming a first layer of a conductive material on a substrate;

forming a first pair of power interconnect lines to distribute power and a second pair of signal interconnect lines to carry signals from the conductive material [interconnect lines from the conductive material];

depositing a first dielectric material over and between the first pair and the second pair [interconnect lines];

forming a mask layer over the first pair and the second pair [interconnect lines] and first dielectric material;

patterning the mask layer such that one portion of the dielectric material between one pair is covered and another portion of the dielectric material between another pair is uncovered [a first portion of the interconnect lines and first dielectric

material are covered, and a second portion of the interconnect lines and first dielectric material are uncovered];

removing the portion of the dielectric material that is uncovered [first dielectric material from the uncovered portion];

removing the patterned mask layer; and

depositing a second dielectric material having a different dielectric constant than a dielectric constant of the first dielectric material.

21. (Amended) The method of Claim 20 [21], wherein the first dielectric material has a dielectric constant greater than a dielectric constant of the second dielectric material.

22. (Amended) The method of Claim 20 [21], wherein the first dielectric material has a dielectric constant less than a dielectric constant of the second dielectric material.

23. (Amended) A method of making in-plane decoupling capacitors, comprising:

forming a first plurality of conductive power lines on an insulating substrate, the first plurality of conductive power lines having a first dielectric therebetween; and

forming a second plurality of conductive signal lines on the insulating substrate, the second plurality of conductive signal lines having a second dielectric therebetween;

wherein the first dielectric has a dielectric constant greater than a dielectric constant of the second dielectric.

24. (Amended) A method of forming an interconnect structure, comprising:

forming, on a substrate, a first plurality of signal interconnect lines and a first intralayer dielectric disposed between the first plurality of signal interconnect lines;

removing a portion of the first intralayer dielectric;

forming a second intralayer dielectric on the substrate where the first intralayer dielectric was removed; and

forming a second plurality of power interconnect lines in the second intralayer dielectric.

25. Claim 25 remains unchanged.

26. (Amended) The method of Claim 25, wherein forming the second plurality of power interconnect lines comprises etching trenches in the second intralayer dielectric, depositing a conductive material, and polishing the conductive material such that the conductive material is substantially removed except for that which is in the trenches.

27. (Amended) A method of forming an interconnect structure, comprising:

forming a first dielectric layer on a substrate;

removing a portion of the first dielectric layer;

forming a second dielectric layer on the substrate where the portion of the first dielectric layer was removed; and

forming a plurality of signal lines in the first dielectric layer and a power line in the second dielectric layer [a plurality of interconnect lines in the first and second dielectric layers].

28. Claim 28 remains unchanged.

29. (Amended) The method of Claim 28, wherein forming the plurality of signal lines and the power line [interconnect lines] comprises etching trenches in the first and the second dielectrics, depositing a conductive material, and polishing the conductive material such that the conductive material is substantially removed except for that which is in the trenches.

Claims 30 - 44 are new.